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APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

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TITLE OF INVENTION: USING DATA COMPRESSION FOR FASTER TESTING OF EMBEDDED MEMORY

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

USING DATA COMPRESSION FOR FASTER TESTING OF EMBEDDED MEMORY

FIELD OF THE INVENTION

The invention relates generally to integrated circuits with embedded memory and, more particularly, to testing the embedded memory.

BACKGROUND OF THE INVENTION

In order to achieve a fast product ramp up and a high yield, any standard memory, for example a standard DRAM or embedded DRAM circuit needs intensive testing. A DRAM typically includes redundant wordlines and bitlines, which can be used to repair defective wordlines and bitlines. Most conventional DRAM testing procedures are designed to find all possible storage cell failures. An external tester collects all of the detected failures into a so-called fail bit map. The external tester uses the fail bit map to determine the best use of the aforementioned on-chip redundancy to repair the detected defects.

The interface between an external tester and a DRAM chip (or a chip having an embedded DRAM) has two major limitations. One limitation is the maximum clock frequency that an external tester can apply to the chip, and the other limitation is the number of pins on the chip that are available for use by the external tester. When testing an embedded memory such as an embedded DRAM, the aforementioned pin limitation is the major problem. For example, today's technologies provide very large and wide embedded DRAMs (e.g. up to 32 Mb with a 256 bit data with). The testing of such

embedded memory circuits is increasingly becoming the most significant cost driving factor in the total chip cost.

FIGURE 1 illustrates a conventional example of testing a DRAM embedded within an integrated circuit, for example an application specific integrated circuit (ASIC). The example of FIGURE 1 illustrates a 64 bit DRAM data bus and a 16 bit wide external tester interface. The timing diagram of FIGURE 1 illustrates a sequence of read accesses of the embedded DRAM, simplified by only showing the column address (CADD) used to access the DRAM. As mentioned above, the embedded DRAM of the FIGURE 1 example has a 64 bit data bus (designated as DQ[63:0]) and, in order to lower the number of pins required for external tester access, the internal 64 bit data bus is multiplexed onto a 16 bit external tester interface (DQ_EXT1[15:0]). Accordingly, four clock cycles of the internal DRAM clock (CLK_INT) are required for the external tester to read out all 64 data bits produced by a single read access of the embedded DRAM. Because the embedded DRAM needs only one cycle of CLK_INT to perform its 64 bit read access, the DRAM remains in an idle mode for the remaining three cycles of CLK_INT required for the external tester to read out all 64 bits.

Another conventional example is illustrated in FIGURE 2. In the example of FIGURE 2, the activity on the 64 bit DRAM data bus DQ and on the external tester interface DQ_EXT1 is the same as in FIGURE 1. However, in the example of FIGURE 2, the embedded DRAM remains in the idle state for seven cycles of CLK_INT, because the frequency of CLK_INT is twice that of the external tester clock CLK_EXT. In contrast, in the example of FIGURE 1, the external tester clock CLK_EXT has the same

frequency as the internal clock CLK_INT of the embedded DRAM. The example of FIGURE 2 illustrates that the DRAM can easily operate internally at higher clock frequencies than the highest clock frequency which can be applied by the external tester, this latter external tester clock frequency being limited by factors such as wire, pad and probe needle parasitic (R, L, C). As shown in FIGURE 2, even though the embedded DRAM can operate at twice the clock frequency of the external tester, the output data rate at DQ_EXT1 is still limited by the clock CLK_EXT of the external tester. The difference caused by the higher internal clock frequency of FIGURE 2 is that the DRAM must remain in its idle mode for seven internal clock cycles between each read access cycle.

The 64-to-16 bit multiplexing and corresponding idle cycles illustrated in FIGURES 1 and 2 disadvantageously limit the speed with which memory testing can be accomplished. This is true whether the internal memory clock has the same frequency or a substantially higher frequency than the test interface clock.

It is therefore desirable to reduce the time required to test embedded memory circuits.

The present invention reduces the time required to test embedded memory circuits by identifying a group of locations within a memory, and compressing the failure information associated with those locations. If the compressed failure information indicates a failure associated with any one of the group of memory locations, then a group of redundant memory circuits respectively associated with the group of memory locations is replaced. Such use of compressed failure information advantageously provides a reduction in the time required for testing an embedded memory circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURES 1 and 2 are timing diagrams which illustrate examples of conventional embedded memory circuit testing.

FIGURE 3 diagrammatically illustrates exemplary embodiments of a global compression circuit for use in embedded memory testing according to the invention.

FIGURE 4 diagrammatically illustrates exemplary embodiments of the local compression circuits of FIGURE 3.

FIGURE 5 diagrammatically illustrates an exemplary implementation of the local compression circuit of FIGURE 4.

FIGURE 6 diagrammatically illustrates an embedded memory testing arrangement according to the invention.

FIGURES 7 and 8 are timing diagrams which illustrate exemplary embedded memory testing operations according to the invention.

FIGURE 9 illustrates exemplary operations which can be performed by the testing arrangement of FIGURE 6.

DETAILED DESCRIPTION

FIGURE 3 diagrammatically illustrates exemplary embodiments of a global compression circuit 101 for use in embedded memory testing according to the invention. In the exemplary embodiments of FIGURE 3, the global compression circuit 101 is coupled to an address bus and a data bus of a memory circuit, thereby to receive address information used by the memory circuit and data stored in the memory circuit. The global compression circuit 101 is also connected to receive expected data, which will be compared to the data received from the memory data bus. The aforementioned address, data and expected data information received by the global compression circuit 101 is indicated generally at 31 in FIGURE 3.

In some embodiments, the memory data bus is 64 bits wide, so the circuit 101 can receive 64 data bits from the memory data bus. These 64 data bits can, for example, correspond to a 64-row x 1 column portion of a memory array (for example a DRAM array) implemented by the memory circuit. Each of the 64 received data bits is input to a respective one of 64 local compression circuits 102, together with the corresponding expected data bit. Each local compression circuit 102 compares its received data bit with the corresponding expected data bit to produce a failure bit that is indicative of whether or not a failure has occurred for that particular memory cell. Each local compression circuit 102 stores the failure bit associated with the memory data bit that it has received. Thereafter each of the 64 local compression circuits 102 receives another memory data bit (e.g. from another 64 row x 1 column portion adjacent to the 64 row x 1 column portion from which the previous memory data was received) along with its corresponding

expected data bit, whereupon the local compression circuit compares the memory data bit to the expected data bit to produce another failure bit which it stores in the same fashion as described above. The 64 local compression circuits 102 repeat this compare and store process for a predetermined number of sets of 64 data bits received from the memory, wherein each set of 64 data bits can be, as described above, a 64 row x 1 column portion of the memory array.

Once the 64 local compression circuits 102 have performed the aforementioned data/expected data compare and failure bit storage operations for a desired number of sets of memory data bits (each set being, for example, a 64 row x 1 column portion) received from the memory circuit, each local compression circuit 102 compresses the stored failure bits into a single bit. Thus, the global compression circuit 101 of FIGURE 1 provides a 64 bit output that represents the test results for K x 64 memory cells of the memory circuit, where K is the number of 64-bit sets of memory data (e.g. the number of columns) to which have been applied the aforementioned data/expected data compare and failure bit storage operations. Thus, the factor K represents the compression factor implemented by the global compression circuit 101.

FIGURE 4 diagrammatically illustrates exemplary embodiments of the local compression circuits 102 of FIGURE3. In FIGURE 4, a data comparator 201 performs the aforementioned data/expected data comparison, and a data multiplexer 202 routes the comparison result to a selected one of a plurality of data latches 203 for storage in the selected data latch. In the embodiments illustrated in FIGURE 4, the data multiplexer 202 is controlled by the least significant three column address bits (CADD (2:0)) of a

DRAM. Thus, as the column address bits sequentially cycle through eight column addresses associated with eight adjacent columns of the memory array, eight data bits (from the respective eight columns) and their corresponding expected data bits are compared in a sequence of eight compare operations at 201, and the resulting eight comparison results (failure bits) are sequentially routed through the data multiplexer 202 into respective ones of the eight data latches illustrated at 203. Thus, FIGURE 4 illustrates embodiments wherein the aforementioned compression factor K = 8.

After the eight failure bits are stored in their data latches 203, these stored failure bits are then compared by a data comparator 204 to produce a final compressed bit which is then stored in a data latch 206. The data latch 206 thus stores a compressed data bit that represents test results for the eight data bits sequentially received at comparator 201 as the column address sequences through eight adjacent columns of the DRAM. Thus, in this example, each of the 64 data bits produced by the 64 local comparator circuits 102 of FIGURE 3 represents compressed test results associated with eight different memory cells in eight adjacent columns of a single row of the memory array. Therefore, the 64 bits of compressed data output by the global compression circuit 101 of FIGURE 1 represent, for example, the test results for 64 groups of eight adjacent memory cells (corresponding, for example, to the cells of a 64 x 8 portion of the memory array).

FIGURE 5 diagrammatically illustrates an exemplary implementation of the local compression circuit 102 of FIGURES 3 and 4. In the embodiment of FIGURE 5, the data comparator 201 is implemented as an exclusive -OR gate which receives the memory bit at 51 and the corresponding expected bit at 52. The data multiplexer 202 is implemented

in FIGURE 5 by inverters 202A, NAND gates 202B and NOR gates 202C interconnected as shown. The data latches 203 are implemented in FIGURE 5 as D flip-flops whose D inputs are driven by the respective NOR gates 202C. The data comparator 204 is implemented in FIGURE 5 by four two-input NOR gates 204A whose respective outputs drive the inputs of a NAND gate 204B (thereby forming an 8-input OR gate). Each NOR gate 204A is driven by the Q outputs of two of the D flip-flops 203. Any logic one stored in any flip-flop 203 (corresponding to a failure detected by exclusive-OR gate 201) will cause NAND gate 204B to output a logic one.

The data latch 206 is implemented in FIGURE 5 by a multiplexer 206A having an output that drives the D input of a D flip-flop 206B. The multiplexer 206A has inputs driven respectively by the NAND gate 204B and the Q output of the flip-flop 206B. The Q output of the flip-flop 206B is the compressed data bit output of the local compression circuit 102. The multiplexer 206A is controlled by a COMPARE signal such that the Q output of flip-flop 206B is fed back to the D input of flip-flop 206B except when the COMPARE signal is active. While the COMPARE signal is active, the output of NAND gate 204B is applied to the D input of the flip-flop 206B. The flip-flops 203 and 206B of FIGURE are all clocked by the internal clock CLK_INT of the embedded memory circuit, and all flip-flops are resettable via signal RESETn.

FIGURE 6 diagrammatically illustrates an exemplary embedded memory circuit testing arrangement according to the invention. The global compressor circuit 101 of FIGURE 1 receives data and address information from an embedded memory circuit 60 along with expected data information (not shown in FIGURE 6). The compressor at 101

outputs the compressed failure bits to a multiplexer 61 which is controlled by a test interface control signal in conventional fashion to multiplex the 64 compressed failure bits onto 16 bits of the external tester interface. An external tester 62 (IC pin boundary is shown by broken line 69) utilizes the compressed failure bits to determine the optimal replacement strategy for the bitlines in the memory circuit 60. The external tester 62 then provides replacement information at 65 to an on-chip replacement handler 63. The replacement handler can use conventional techniques to produce at 66 control signaling which causes the memory circuit 60 to replace the bitlines associated with any of the 64 groups of K memory cells represented by the 64 compressed failure bits. For example, the external tester 62 may direct the replacement handler 63 to replace all bitlines associated with any group whose corresponding compressed failure bit is a logic one (indicating failure of at least one of the K cells in the group).

Also as shown in FIGURE 6, the memory circuit 60 is coupled for bidirectional communication with one or more data processors 67 embedded within the same integrated circuit as the memory circuit 60, as is common in ASIC designs.

FIGURE 7 is a timing diagram which illustrates exemplary operations that can be performed by the embodiments of FIGURES 3-6. In the example of FIGURE 7, the frequency of the internal memory clock CLK_INT is twice the frequency of the external tester clock CLK_EXT. This permits the 64 bit data bus of the embedded memory circuit to be accessed eight times during the amount of time (four external tester clock cycles) required to multiplex 64 compressed failure bits (DQ_CMPR) onto the 16 bit external tester interface at DQ_EXT6. Thus, the example of FIGURE 7 illustrates operation of

the specific implementation shown in FIGURES 4 and 5, wherein K = 8 and eight data latches 203 are provided for respectively storing the results of eight successive data/expected data compares. The COMPARE signal (see also FIGURE 5) is active during every eighth cycle of CLK_INT to permit the output of comparator 204 (see FIGUREs 4 and 5) to be latched at 206. The signal DQ_EXP represents the 64 expected data bits corresponding to the 64 data bits from the internal memory data bus DQ[63:0]. The signals illustrated in FIGURE 7 are also labeled at selected points where they appear in FIGURES 3-6.

FIGURE 8 is a timing diagram which illustrates further exemplary memory testing operations according to the invention. FIGURE 8 is similar to FIGURE 7, but in the example of FIGURE 8, the internal memory clock CLK_INT has the same frequency as the external tester clock CLK_EXT, so the 64 bit internal memory data bus can be read four times in the amount of time required to multiplex 64 bits onto the 16-bit external tester interface. Thus, in this example, the compression factor K = 4. For this example, the local compression circuits 102 of FIGURES 4 and 5 would require only a 4-way multiplexer 202 and four data latches 203, and only the least significant two bits of the column address CADD would be needed to control the multiplexer 202.

From the foregoing description, it can be seen that the compression factor K depends on the frequency relationship between the internal memory clock CLK_INT and the external tester clock CLK_EXT. At higher frequencies of CLK_INT, a higher compression factor K can be achieved, although a wider multiplexer and more data latches are required in each local compression circuit. As illustrated in FIGURES 7 and

8, the amount of time required for testing an embedded memory circuit is directly related to the compression factor K (K = 8 in FIGURE 7 and K = 4 in FIGURE 8). Thus, the operation of FIGURE 7 reduces the test time by a factor of 8 and the operation of FIGURE 8 reduces the test time by a factor of 4.

FIGURE 9 illustrates exemplary operations which can be performed by the embodiments of FIGURES 3-6. The exemplary operations of FIGURE 9 assume a compression factor of K and an N-bit wide internal memory data bus. At 91, bit failure information is compressed for N groups of K memory cells each. At 92, all groups whose associated compressed bit failure information indicates a failure are identified. At 93, all bitlines of any group identified at 92 are replaced. Thereafter, the operations at 91-93 are repeated.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.